Remarks

The instant office action dated September 5, 2008 indicates that: claim 14 stands rejected under 35 U.S.C. § 101; claims 1-10 and 12-13 stand rejected under 35 U.S.C. § 103(a) over Tanaka (US Patent No. 4,733,346) in view of Gupta (US Patent No. 5,996,083); and claim 11 stands objected to but is indicated as allowable if rewritten. Applicant traverses all of the rejections and objections, unless explicitly stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Office Action.

The Section 103(a) rejections are improper because the combination of the '346 and '083 references does not teach or suggest all claim limitations as asserted, including those directed to disabling register banks via the gating of clock inputs. Specifically, the Office Action has erroneously equated the blocking of CPU access to a particular register with the claimed disabling of the register, but the '346 reference does not disclose "gating off the address and data inputs" of a register file as asserted at page 3 of the Office Action. For instance, the cited portion of the '346 reference at column 8:66-67 involves preventing access to a register block in a particular state "C" as discussed in the Office Action, but this access prevention makes no mention of disabling a register block as claimed (*e.g.*, shutting down the block to preserve power). Moreover, there is no discussion of gating off address and data inputs of such a register, either at the cited portions of column 8 or at the further cited portions of column 10. In other words, while the '346 reference discusses preventing the CPU 10 from accessing a register set in state "C," a register in such a state has received a reset signal, is set at a "0" level, and is active to receive further inputs. Referring to column 9:58-65 of the '346 reference, output signals "of a '0' level are generated from the Q output terminals of the flip-flop circuits 50 to 52 in the state control circuit 18C, thereby setting the register block 12C in state 'C'." The register is accordingly not disabled and, instead, is ready to receive further signals for operation in different states. Accordingly, the '346 reference cannot operate "by gating off the address and data inputs" and fails to disclose the same.

The Office Action has also erroneously equated the disabling of functional units, which carry out specific functions based upon software instructions, with the claimed disabling of a bank in a register file (*e.g.*, that stages data between memory and functional

units). For instance, the cited power control settings and gated clock signal from the '083 reference discuss gating a clock signal for functional units within a microprocessor (*i.e.*, units that carry out specific tasks or functions). As described at cited column 3:40-63, functional units such as "branch prediction hardware" or an "external bus interface" are selectively disabled based upon whether the specific functions carried out by the unit are "required by the currently executing software." This "offloads the task of dynamically sensing and decoding instruction activity from the hardware to the software." The "power control register" as discussed in the Office Action is therefor not selectively disabled. Rather, the power control register must remain functional as it is used to store information for selectively disabling the functional units. In this context, the cited '346 reference does not teach gating clock inputs to register banks (as indicated at page 3 of the Office Action), and the '083 reference's function-specific approach to selectively disabling hardware functions is unrelated to the claimed disabling of a bank that stores information independently from any such task. Accordingly, the Office Action has failed to show correspondence to the claim limitations directed to the selective disabling of a register file bank.

The proposed combination of references is also in violation of Section 103(a) because modifying the primary '346 reference to completely disable a register bank would result in an inoperable system. For instance, the '346 reference cannot operate "by gating off the address and data inputs" of the cited register set to state "C" because the register would no longer function to receive inputs, and would accordingly be inoperable for its intended purpose. The proposed combination is also in violation of Section 103(a) because effectively disabling the cited "power control register" from the '083 reference would render the register inoperable, meaning that the register can no longer control the operation of functional units to reduce power consumption. That is, the proposed combination would fail to achieve the indicated purpose of the combination.

Claim 11 has been amended to independent form, to include the limitations of independent claim 1 and intervening claims 8 and 9, from which claim 11 had depended. Based upon the Office Action's indication, Applicant understands that claim 11 is in condition for allowance.

Claim 14 has been amended to remove the term "signal bearing" in accordance with the Examiner's suggestion. Claim 14 now recites a "recordable medium" as bearing a hardware definition program. Accordingly, Applicant believes that the Section 101 rejection is no longer applicable.

Claims 3 and 17 have been amended to include limitations directed to gating off clock, address and data inputs to block all pertinent clock, address and data signals to the bank. These amendments are believed to be consistent with the claims as previously presented, and are supported in various portions of the specification (*see, e.g.*, FIG. 3 and corresponding discussion at paragraph 55). Applicant believes the amended claims to be allowable for reasons discussed above, and further because the cited references fail to teach or suggest blocking all clock, address and data inputs to a register file bank.

Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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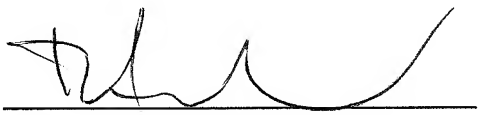
By: 

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